

**IN THE CLAIMS:**

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1           1.       (Currently Amended) A data processor comprising:  
2                   C execution clusters, each of said C execution clusters comprising an instruction  
3       execution pipeline having N processing stages capable of executing instruction bundles comprising  
4       from one to S syllables, wherein each of said instruction execution pipelines is L lanes wide, each  
5       of said L lanes capable of receiving one of said one to S syllables of said instruction bundles;  
6                   an instruction cache capable of storing a plurality of cache lines, each of said cache  
7       lines comprising C\*L syllables;  
8                   an instruction issue unit capable of receiving fetched ones of said plurality of cache  
9       lines and issuing complete instruction bundles toward said C execution clusters; and  
10                  alignment and dispersal circuitry capable of receiving said complete instruction  
11       bundles from said instruction issue unit and routing each of said received complete instruction  
12       bundles to a correct one of said C execution clusters as a function of at least one address bit  
13       associated with each of said complete instruction bundles.

1           2.       (Currently Amended) The data processor as set forth in Claim 1 wherein said  
2 alignment and dispersal circuitry ~~routes~~ routes each of said received complete instruction bundles to  
3 said correct execution cluster as a function of at least one address bit associated with at least one  
4 syllable in each of said ~~each~~ complete instruction ~~bundle~~ bundles.

1           3.       (Currently Amended) The data processor as set forth in Claim 1 wherein said  
2 alignment and dispersal circuitry routes each of said received complete instruction bundles to said  
3 correct execution cluster as a function of a cluster bit associated with each of said complete  
4 instruction ~~bundle~~ bundles.

1           4.       (Currently Amended) The data processor as set forth in Claim 1 wherein said  
2 alignment and dispersal circuitry ~~routes~~ routes each of said received complete instruction bundles to  
3 said correct execution cluster as a function of a stop bit associated with at least one syllable in each  
4 of said ~~each~~ complete instruction ~~bundle~~ bundles.

1           5.       (Currently Amended) The data processor as set forth in Claim 1 wherein said  
2 alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said ~~each~~  
3 received complete instruction ~~bundle~~ bundles to any one of said C execution clusters.

1           6.       (Original) The data processor as set forth in Claim 5 wherein said alignment and  
2       dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry.

1           7.       (Currently Amended) The data processor as set forth in Claim 6 wherein said control  
2       logic circuitry controls said multiplexer circuitry as a function of at least one of:

3                   1) said at least one address bit associated with each of said ~~each~~ complete instruction  
4       ~~bundle~~ bundles;

5                   2) at least one address bit associated with at least one syllable in each of said ~~each~~  
6       complete instruction ~~bundle~~ bundles; and

7                   3) a cluster bit associated with each of said ~~each~~ complete instruction ~~bundle~~ bundles.

1           8.       (Original) The data processor as set forth in Claim 1 wherein  $L=4$ .

1           9.       (Original) The data processor as set forth in Claim 1 wherein  $C=3$ .

1           10.      (Currently Amended) A processing system comprising:

2                   a data processor;

3                   a memory coupled to said data processor;

4 a plurality of memory-mapped peripheral circuits coupled to said data processor for  
5 performing selected functions in association with said data processor, wherein said data processor  
6 comprises:

7 C execution clusters, each of said C execution clusters comprising an  
8 instruction execution pipeline having N processing stages capable of executing instruction  
9 bundles comprising from one to S syllables, wherein each of said instruction execution  
10 pipelines is L lanes wide, each of said L lanes capable of receiving one of said one to S  
11 syllables of said instruction bundles;

12 an instruction cache capable of storing a plurality of cache lines, each of said  
13 cache lines comprising C\*L syllables;

14 an instruction issue unit capable of receiving fetched ones of said plurality of  
15 cache lines and issuing complete instruction bundles toward said C execution clusters; and

16 alignment and dispersal circuitry capable of receiving said complete  
17 instruction bundles from said instruction issue unit and routing each of said received  
18 complete instruction bundles to a correct one of said C execution clusters as a function of at  
19 least one address bit associated with each of said complete instruction bundles.

1           11.     (Currently Amended) The processing system as set forth in Claim 10 wherein said  
2 alignment and dispersal circuitry ~~routes~~ routes each of said received complete instruction bundles to  
3 said correct execution cluster as a function of at least one address bit associated with at least one  
4 syllable in each of said ~~each~~ complete instruction ~~bundle~~ bundles.

1           12.     (Currently Amended) The processing system as set forth in Claim 10 wherein said  
2 alignment and dispersal circuitry ~~routes~~ routes each of said received complete instruction bundles to  
3 said correct execution cluster as a function of a cluster bit associated with each of said ~~each~~ complete  
4 instruction ~~bundle~~ bundles.

1           13.     (Currently Amended) The processing system as set forth in Claim 10 wherein said  
2 alignment and dispersal circuitry ~~routes~~ routes each of said received complete instruction bundles to  
3 said correct execution cluster as a function of a stop bit associated with at least one syllable in each  
4 of said ~~each~~ complete instruction ~~bundle~~ bundles.

1           14.     (Currently Amended) The processing system as set forth in Claim 10 wherein said  
2 alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said ~~each~~  
3 received complete instruction ~~bundle~~ bundles to any one of said C execution clusters.

1           15.    (Original) The processing system as set forth in Claim 14 wherein said alignment and  
2   dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry.

1           16.    (Currently Amended) The processing system as set forth in Claim 15 wherein said  
2   control logic circuitry controls said multiplexer circuitry as a function of at least one of:

3                   1) said at least one address bit associated with each of said ~~each~~ complete instruction  
4   ~~bundle~~ bundles;

5                   2) at least one address bit associated with at least one syllable in each of said ~~each~~  
6   complete instruction ~~bundle~~ bundles; and

7                   3) a cluster bit associated with each of said ~~each~~ complete instruction ~~bundle~~ bundles.

1           17.    (Original) The processing system as set forth in Claim 10 wherein  $L=4$ .

1           18.    (Original) The processing system as set forth in Claim 10 wherein  $C=3$ .

1           19.     (Currently Amended) For use in a data processor comprising C execution clusters,  
2     each of the C execution clusters comprising an instruction execution pipeline having N processing  
3     stages capable of executing instruction bundles comprising from one to S syllables, wherein each  
4     of the instruction execution pipelines is L lanes wide, each of the L lanes capable of receiving one  
5     of the one to S syllables of the instruction bundles, a method of routing instruction bundles into the  
6     L lanes in the C execution clusters comprising the steps of:

7                   fetching cache lines from an instruction cache, each of the cache lines comprising  
8     C\*L syllables;

9                   issuing complete ~~ones of the~~ instruction bundles toward the C execution clusters; and  
10                   routing each of the received complete instruction bundles to a correct one of the C  
11     execution clusters as a function of at least one of:

12                   1) ~~the~~ at least one address bit associated with each of the ~~each~~ complete  
13     instruction ~~bundle~~ bundles;

14                   2) at least one address bit associated with at least one syllable in each of the  
15     ~~each~~ complete instruction ~~bundle~~ bundles; and

16                   3) a cluster bit associated with each of the ~~each~~ complete instruction ~~bundle~~  
17     bundles.

1           20.    (Original) The method as set forth in Claim 19 wherein  $L=4$  and C.

1           21.    (New) The data processor as set forth in Claim 1, wherein said alignment and  
2   dispersal circuitry is further capable of aligning said syllables with correct ones of said lanes.

1           22.    (New) The processing system as set forth in Claim 10, wherein said alignment and  
2   dispersal circuitry is further capable of aligning said syllables with correct ones of said lanes.